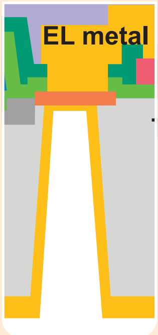
FOUNDRY INNOVATION BY UMS

At UMS we constantly innovate to make our open III-V foundry technologies more and more efficient for our customers, facilitating frequency rise and assembly in innovative ad-hoc solutions (BGA, etc.).
Check out our new generations PH10-20 and PH25-20.

I.S.V.

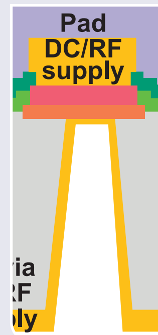


Individual Source Vias

Thanks to thinner substrate, FET via-holes for grounding can be directly below FET sources to reduce parasitic source inductance. The FET is more compact:

- Higher Ft, Fmax
- Higher Gain
- Easier matching

H.V.

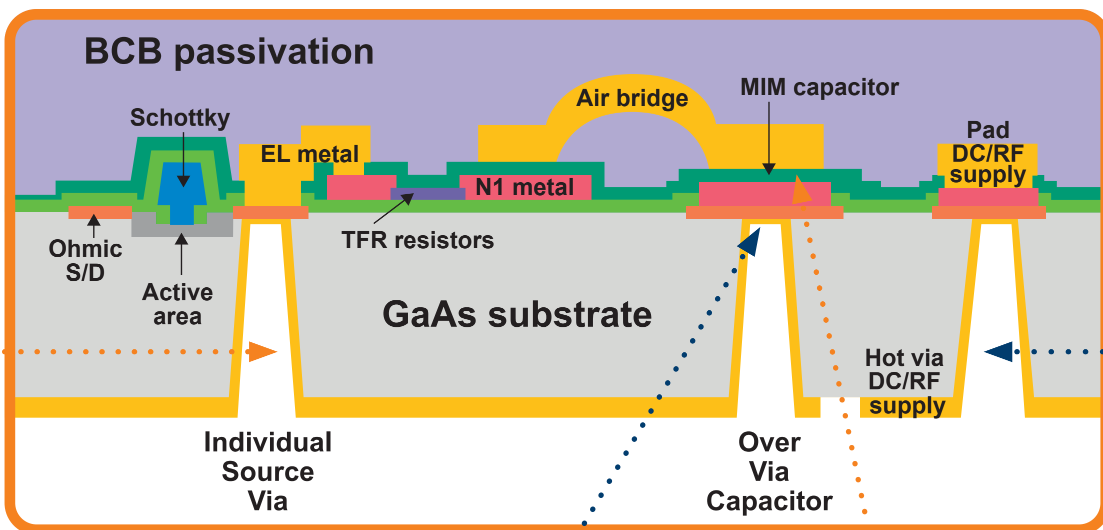


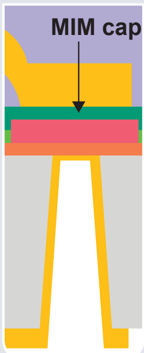
Hot Vias

That new option allows RF signal or DC biasing to be handled through a back side patterning.

Die may be assembled with a flip-chip process in BGA solutions, shortening connections for DC & RF.

Very efficient solution for high frequency MMICs, reducing the parasitics of assembly (no more long wires needed).



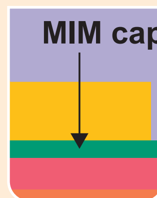


C.O.V.

Capacitor over Via

Small via-holes directly connected to the bottom electrode of shunt MIM capacitor make it better for high frequency design, strongly reducing the series inductance:

Design is more compact and efficient, wideband design is also simplified.



H.D.M.C.

High density MIM Capacitor

Specific dielectric layers, optimized to support high voltages, define two capacitor density options.

In particular, the new 625pF/mm² capacitor density allows more compact design by significantly reducing the size of the decoupling network.

United Monolithic Semiconductors

Build your own solution with UMS

www.ums-rf.com